REMARKS

Claims 1-9 and 27-30 are pending and were finally rejected. Claims 1, 8, 27 and 28 have been amended herein. Claims 10-27 were previously withdrawn. No new matter has been added.

Applicant has amended each of the pending independent claims in a manner that is believed to overcome the prior art references without requiring further search or examination. Accordingly, withdrawal of the final rejection and allowance of the claims is respectfully requested.

Claims 1-6 were rejected as being unpatentable over the combination of Lum (U.S. Patent No. 5,696,931, hereinafter "Lum") over Hicken (U.S. Patent No. 6,092,149, hereinafter "Hicken"). Claim 1 has been amended to clarify that two things occur substantially concurrently: (1) auto-transfer of requested data from the cache to the host; and (2) request to transfer data from the mass storage device <u>directly</u> to the host. None of the cited references teach or suggest transferring requested data directly to the host in this manner.

In the "Response to Arguments" section of the last Office Action, Examiner asserted that Hicken unequivocally discloses "coalescing commands or executing internal commands in parallel; Abstract; maximizing performance through the execution of internal processes in parallel which include receiving a plurality of commands from the host including a read command for cached data and transferring data from the cache to the host; col. 2 ll 35-59."

The cited portion of Hicken makes clear, however, that Hicken is describing transferring data <u>from the cache to the host.</u> Nothing in Hicken teaches or suggests concurrently transferring data directly from the mass storage device to the host. In fact, Hicken further states in the same

paragraph that "steps 420 and 422 may be performed multiple times <u>during the transferring data into the disc cache</u> so as to allow the transfer of data to the Host" (col. 9, lines 10-13, emphasis added). Clearly, Hicken is describing a transfer of data to the cache and from the cache to the host. This is a substantially different mode of operation than Applicant's claimed limitation of transferring data from the mass storage device "directly" to the host. Because a substantially different instruction set would be required and interface with a disc controller (as opposed to communication with the cache) would be required, it would not have been obvious to modify Hicken to achieve transferring "directly" absent Applicant's own teaching. Furthermore, and as discussed below with reference to claim 8, Lum also fails to teach or suggest this claim limitation. Hence, claim 1 (and by dependence claims 2-7) are patentably distinct over Lum and Hicken, individually or in combination.

Claim 8 was rejected as being unpatentable over Lum over Simionescu (U.S. Patent No. 6,141,728, hereinafter "Simionescu"). Claim 8 has, likewise, been amended to clarify that if a portion of the requested data is in the cache memory and a portion is in the mass storage device, then two things occur substantially concurrently: (1) transferring the portion of the requested data from the cache memory to the host system; and (2) transferring the portion of the requested data from the mass storage device <u>directly</u> to the host system. Again, the cited references fail to teach or suggest this limitation.

In the Response to Arguments section of the last Office Action, Examiner asserted that "Lum clearly discloses '<u>transferring of data into the disc cache</u> so as to allow the transfer of data to the host to start <u>before</u> (hence concurrent with) the last of the requested data is stored in the disc cache 118'" (some emphasis in original, some emphasis added). The cited portion demonstrates that Lum merely discloses transferring data "into the disc cache," and does not

disclose or suggest transferring data "from the mass storage device directly to the host system," as required by claim 8.

Examiner also cited to Lum for the proposition that, "when there is a partial software cache hit, the microprocessor instructs the disc interface <u>to transfer the data</u> requested in Host command that is not in disc cache, plus 'n' additional subsequent sectors <u>to the disc cache</u>; col. 9 ll 1-55" (emphasis added). Again, this cited portion demonstrates that Lum discloses a different system in which data is being transferred to the cache, and does not disclose a system in which data is being substantially concurrently transferred directly from the mass storage device <u>directly</u> to the host. As such, Lum teaches away from the novel combination of elements recited by claim 8.

Simionescu also fails to teach or suggest a system in which data is being substantially concurrently transferred directly from the mass storage device <u>directly</u> to the host. In the Response to Arguments section, Examiner asserted that Simionescu discloses, "at the same time, firmware causes the disk drive to read additional sectors <u>from the disk into the cache buffer</u>, and these additional sectors are located during rescanning and are thereupon automatically transferred to the host; in col. 21 ll 10-26." Again, like Lum and Hicken, Simionescu merely discloses transferring data from the disk drive into the cache. Simionescu does not disclose the claimed limitation of "transferring the portion of the requested data from the cache memory to the host system substantially concurrently with transferring the portion of the requested data from the mass storage device <u>directly</u> to the host system," as required by claim 8 (emphasis added).

Because neither Lum nor Simionescu, either alone or in combination, teaches the recited claim limitation, claim 8 is patentably distinct over the cited references.

Claims 27-28 and 30 were also rejected over Lum over Simionescu. Claim 27 (and by dependence claims 28 and 30) has also been amended to clarify that the system will, "concurrently cause said disk-controller to auto-transfer said cache-hit-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said cache-miss-portion of said data-request directly from said disk-device" (emphasis added). As discussed above, neither Lum nor Simionescu teach or suggest this limitation. Rather, the cited references merely disclose transferring data from a disk drive to a cache and also transferring data from the cache to the host. The recited claim limitation distinguishes over that teaching.

Claim 7 was rejected as being unpatentable over Lum in view of Hicken and in view of "well-known practices in the art." Claim 7 depends from claim 1 as is patentably distinct over the cited art for the reasons provided above with regard to claim 1 as well as for its further defining limitations. Nothing in "well-known practices in the art" is sufficient to overcome the above-described deficiencies in Lum and Hicken. Hence, claim 7 is allowable.

Claim 29 was rejected as being unpatentable over Lum in view of Simionescu and in view of "well-known practices in the art." Claim 29 depends from 28 as is patentably distinct over the cited art for the reasons provided above with regard to claim 28 as well as for its further defining limitations. Nothing in "well-known practices in the art" is sufficient to overcome the above-described deficiencies in Lum and Simionescu. Hence, claim 29 is allowable.

Claim 9 was rejected as being unpatentable over Lum in view of Simionescu and in view of Taroda (U.S. Publication No. 201/10014929, hereinafter "Taroda"). Claim 9 depends from 8 as is patentably distinct over the cited art for the reasons provided above with regard to claim 28

as well as for its further defining limitations. Nothing in Taroda is sufficient to overcome the above-described deficiencies in Lum and Simionescu. Hence claim 9 is allowable.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner please contact Applicants' attorney at the address below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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